AMENDMENT(S) TO THE SPECIFICATION

Please replace paragraph [0005] with the following rewritten paragraph:

Referring now to both Figures 1 and 2, each device ~~include~~ includes source regions 10 each formed in a channel region 12. Gate structures are formed adjacent source regions 10 and the channel region 12 in which the source regions 10 are formed. Each gate structure includes a gate electrode 14, which is typically formed from a conductive polysilicon, and a gate insulation layer 16 which is typically comprised of silicon dioxide. Each gate insulation layer 16 insulates its associated gate electrode 14 from an adjacent channel region 12.

Please replace paragraph [0010] with the following rewritten paragraph:

A superjunction structure allows the designers to decrease the Rdson of a device without adversely affecting its breakdown voltage. A superjunction device includes alternating P and N type regions below the active cells of the device. The alternating P and N type regions are in substantial charge balance so that under a reverse voltage condition these regions deplete one another thereby allowing the device to withstand breakdown. Thus, a superjunction arrangement allows for an increase in the conductivity of the drain region to improve the Rdson without an ~~affect~~ effect on the breakdown voltage rating of the device.

Please replace paragraph [0012] with the following rewritten paragraph:

In a superjunction device of a proven given breakdown voltage, it is known that Rdson per unit area is reduced as the width (Wp) of regions 28 and drain region 18 is reduced. Thus, for a device such as the one shown in Figure 2, it is desirable to reduce the pitch (the cell to cell spacing defined by the distance between the center of adjacent ~~trenches~~ gate electrodes in Figure 2 or trenches in Figure 1).

Please replace paragraph [0038] with the following rewritten paragraph:

When an appropriate voltage is applied to the gate electrodes 14 of a device according to the present invention, channels are formed as described earlier connecting respective source

regions 10 to drain columns 30, whereby current may travel from source regions 10, through respective channels to respective drain columns 30 and eventually to drain region [[12]] 18.

Please replace paragraph [0040] with the following rewritten paragraph:

Specifically, trenches 32 are formed in a trench receiving structure such as the one shown by Figure 5A. A trench receiving structure includes substrate 20, and epitaxially formed semiconductor layer 18 of the same conductivity as substrate 18 formed over substrate 20, charge balance region 28 formed adjacent epitaxial layer 18, channel region 12 formed adjacent charge balance region 28, and source region 10 formed over channel region 12. Charge balance region 28, channel region 12 and source region 10 may be formed in epitaxial layer 18 through blanket implantation, or each region may be epitaxially formed. For example, charge balance region 28 may be epitaxially formed over drain region 18, and then doped to ~~formed~~ form channel region 12.

Please replace paragraph [0050] with the following rewritten paragraph:

Figure 6 shows an alternative embodiment of the present invention. In the embodiment shown by Figure 6, first a portion 42 of each drain column 30 is formed in an epitaxial layer 44. Epitaxial layer 44 is formed over drain region 18. Thereafter, a second epitaxial layer 46 is formed over epitaxial layer 44 and a process according to the present invention is followed to form a second portion [[46]] 48 to complete each drain column 30. Epitaxial layers 44, 46 are doped so that they may be in charge balance with drain columns 30.